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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRIER, JEFFERY A	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/642,458	MACINNIS ET AL.	
	Examiner	Art Unit	
	Jeffery A. Brier	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-39,41,49-51,53 and 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-39,41,49-51,53 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 9/30/2005 has been entered.

Response to Arguments

2. Applicant's arguments filed 9/30/2005 have been fully considered but they are not persuasive.

The arguments concerning "MPEP transport stream" have been considered, but, since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPEP transport steams are received by the set-top box which includes the single integrated chip that also decompresses MPEG. Refer to the following definition of set-top box which may be found at http://searchnetworking.techtarget.com/sDefinition/0,,sid7_gci212971,00.html.

set-top box

powered by whatis?com

A set-top box is a device that enables a television set to become a user interface to the Internet and also enables a television set to receive and decode digital television (DTV) broadcasts. DTV set-top boxes are sometimes called receivers. A set-top box is necessary to television viewers who wish to use their current analog television sets to receive digital broadcasts. It is estimated that 35 million homes will use digital set-top boxes by the end of 2006, the estimated year ending the transition to DTV.

In the Internet realm, a set-top box is really a specialized computer that can "talk to" the Internet - that is, it contains

a Web browser (which is really a Hypertext Transfer Protocol client) and the Internet's main program, TCP/IP. The service to which the set-top box is attached may be through a telephone line as, for example, with WebTV, or through a cable TV company like TCI.

In the DTV realm, a typical digital set-top box contains one or more microprocessors for running the operating system, possibly Linux or Windows CE, and for parsing the MPEG transport stream. A set-top box also includes RAM, an MPEG decoder chip, and more chips for audio decoding and processing. The contents of a set-top box depend on the DTV standard used. European DVB-compliant set-top boxes contain parts to decode COFDM transmissions while ATSC-compliant set-top boxes contain parts to decode VSB transmissions. More sophisticated set-top boxes contain a hard drive for storing recorded television broadcasts, for downloaded software, and for other applications provided by your DTV service provider.

Digital television set-top boxes are used for satellite, cable, and terrestrial DTV services. They are especially important for terrestrial services because they guarantee viewers free television broadcasting. A set-top box price ranges from $100 for basic features to over $1,000 for a more sophisticated box. It is often leased as part of signing up for a service.

Last updated on: Sep 05, 2001

In the third paragraph this discussion state the set-top box processes an MPEP transport stream.

Another reference to set-top box and MPEP Transport may be found at http://www.cisco.com/en/US/products/hw/cable/ps328/products_data_sheet09186a0080091ac7.html.

Data Sheet

Cisco 6920 RateMUX
Advanced MPEG-2 Multiplexer

Future-proofing the cable headend with advanced digital video capabilities

Enhanced television—electronic program guides and other "interactive" data can be multiplexed into the MPEG transport for use by the set-top box (STB)

Thus, one of ordinary skill in the art would associate with the set-top box of So the ability to process MPEP transport streams. So discusses set-top box and television set at column 3 lines 35-38 and 58-61, column 129 lines 22-31, and column 134 lines

48-51 and discusses receiving cable broadcast at column 130 lines 33-40. Thus, to one of ordinary skill in the art the MPEG decompression and compression associated with the single chip embodiment of So at least processes MPEG Transport video and audio streams. The function of the MPEG Transport processor is not claimed.

The arguments concerning unified memory are not persuasive because So teaches using unified memory at column 16 lines 62-63 and column 99 lines 58-67 which discuss unified memory as the memory for the whole system, CPU, MPEG decoding, and graphics.

The argument concerning claim 30, see page 17, is not persuasive because the term television includes many television standards including HDTV.

The argument concerning claim 37 and 38, see page 18, and the 103 rejection, see pages 20-22, is not persuasive because column 7 lines 33-59 discusses converting the CPU origin streams to the appropriate endian used in the DSP. One of ordinary skill in the art would have been motivated to modify So to include this feature due to the variety of video sources in So.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35, 36, 39, 41, 50, 51, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by So, U.S. Patent No. 5,909,559.

So teaches integrating a north bridge with a MPEG coder decoder (compression decompression) at column 133 lines 47-67. This section of the patent states:

> Chip 510 has its memory size and pinout tailored for 3D graphics and geometry slope/setup, MPEG compression/ decompression algorithms, and/or 3D audio. Advantageously, CPU 315 is relieved of burden of much of these calculations, and freed from much time-consuming MMX context switching latency. Another embodiment of chip 510 integrates blocks 520 and 525 together with advantageously low real estate and reduced pinout, and PCI/PCI block 530 is a separate chip.
>
> In FIG. 6, another embodiment 600 of an improved computer system is comparable to FIG. 5 except that a north bridge-type block 610 has a first VSP core enhancing the north bridge PCI/MCU circuitry and that first VSP runs 3D geometry and multimedia extensions acceleration. A second VSP block 620 virtualizes 3D audio, graphics, slope/setup and MPEG audio/video compression/decompression. Blocks 610 and 620 are integrated together into a single integrated circuit chip, and both blocks 610 and 620 are coupled to PCI bus 330 as master/slave agents. An accelerator bus 615 couples blocks 610 and 620. PCI/PCI bridge 530 is on or off-chip in different embodiments.

Claim 1:

So teaches a system on a single integrated circuit chip (*column 133 lines 29-67*) comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams (*So teaches applying the integration of the Northbridge and MPEG decompression and compression algorithms to a set-top box which to one of ordinary skill in the art is connected to broadcast cable which by applicants definition MPEG broadcast is MPEG Transport. The only function associated with this processor is receiving which is a broad process met by So's chip receiving the MPEG Transport stream.*), at least one of the MPEG Transport streams including MPEG video data (*Column 133 line 62.*);

an MPEG video decoder for decoding the MPEG video data to generate video using an external memory for displaying (*Column 133 lines 29-67, especially note line 62 which specifically discusses MPEP video decompression which is MPEG decoding. An external memory is used for displaying the generated video.*);

a display engine (graphics elements 126, 315, 345, 350, 510, 520, 525, 620) for processing graphics to be blended (*This is an intended function but not an actual function because blending is actually not occurring.*) with the video using the external memory (*Applicant needs to more concretely claim the elements of 1400 as illustrated in figure 40.*); and

a system bridge controller having a north bridge function disposed between a CPU (*CPU 315*) and a plurality peripheral devices (*Devices listed in block 550 (1394,*

TV, LAN, WAN, ATM), devices connected to south bridge 410, and any devices connected to PCI buses 330 and 540.) for coupling the CPU to the plurality of peripheral devices (*Column 133 lines 29-67, especially note lines 57-58 which discuss north bridge type block 610 which performs north bridge function.*),

wherein the MPEG video decoder , the display engine, and the system bridge controller are implemented on the single integrated circuit chip (*Column 133 lines 29-67, note especially lines 33-38 and 63-65.*), and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (*Figures 5 and 6 and column 133 lines 29-67 clearly teach the CPU and the peripheral devices are external to the integrated circuit 510 shown in figure 5 and integrated circuit chip containing 610 and 630. column 133 lines 41-45 clearly discuses 550 to be separate chips from the chip containing the north bridge and MPEG video decoder.*), and

wherein the external memory has a unified memory architecture (*Column 16 lines 62-63 and column 99 lines 58-67 discuss unified memory as the memory for the whole system, CPU, MPEG decoding, and graphics.*), such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory (*This is interpreted to mean also all of its main memory.*), the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

Claim 41:

So teaches a system on a single integrated circuit chip (*column 133 lines 29-67*) comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams (*So teaches applying the integration of the Northbridge and MPEG decompression and compression algorithms to a set-top box which to one of ordinary skill in the art is connected to broadcast cable which by applicants definition MPEG broadcast is MPEG Transport. The only function associated with this processor is receiving which is a broad process met by So's chip receiving the MPEG Transport stream.*), at least one of the MPEG Transport streams including MPEG video data (*Column 133 line 62.*);

an MPEG video decoder for processing MPEG video data to generate video for displaying (*Column 133 lines 29-67, especially not line 62 which specifically discusses MPEP video decompression which is MPEG decoding.*); and

a system bridge controller having a north bridge function disposed between a CPU (CPU 315) and a plurality peripheral devices (*Devices listed in block 550 (1394, TV, LAN, WAN, ATM), devices connected to south bridge 410, and any devices connected to PCI buses 330 and 540.*) for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices (*Column 133 lines 29-67, especially note lines 57-58 which discuss north bridge type block 610 which performs north bridge function.*),

wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip (*Column*

133 lines 29-67, note especially lines 33-38 and 63-65. The set-top box inherently contains MPEG Transport processor and MPEG video decoder.), and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (*Figures 5 and 6 and column 133 lines 29-67 clearly teach the CPU and the peripheral devices are external to the integrated circuit 510 shown in figure 5 and integrated circuit chip containing 610 and 630. Column 133 lines 41-45 clearly discuses 550 to be separate chips from the chip containing the north bridge and MPEG video decoder.*).

This system claim adds to system claim 1 "an MPEG Transport processor for receiving a plurality of MPEG transport streams, at least one of the MPEG Transport streams including MPEG video data". So discusses two MPEG streams, audio and video, see column 133 line 62. Thus, a transport processor is in the MPEG coder/decoder to allow both streams to be processed.

Claim 5:

Column 133 lines 29-67 discusses the north bridge connecting the CU to the PCI peripheral devices.

Claim 6:

Inherently PCI bus master allows one PCI device to communicate to another PCI device without using CPU as an intermediate device.

Claim 9:

The 550 and 560 are an I/O devices.

Claim 10:

The north bridge 520, 610 allows DMA between CPU 315 and memory 325.

Claim 11:

The north bridge 520 is connected to memory 525 and to any memory connected to the PCI bus.

Claim 14:

The single integrated circuit 510, 610 has a north bridge block 520 that connects the CPU to the MPEG video decoder 525, 620.

Claim 15:

Column 126 line 55 discusses MIPS processor.

Claim 16:

Column 100 lines 34-35 discusses burst in PCI.

Claim 17:

The north bridge inherently has buffers to buffer speed contention between differing devices.

Claim 20:

HDTV means high definition TV which is inferred by referenced to television at column 129 line 31.

Claim 21:

SDTV means standard definition TV which is NTSC TV, PAL TV, and SECAM TV which is discussed at column 129 line 57.

Claim 50:

This claim depends upon claim 9. So discusses attaching an ISA bus along with the PCI bus. The ISA bus (8 bits or 16 bits) has less bits than the PCI bus (32 bits or 64 bits), thus, the north bridge converts CPU data of 32 or 64 bits to ISA bus data of 8 or 16 bits.

Claim 53:

Column 157 line 55 to column 158 line 13 discusses integrating all of the components except for CPU and memory onto a single integrated circuit. This application is directed to multimedia and web applications thus it teaches compositing graphics and MPEG and since it has a single integrated circuit teaching the patent teaches to one of ordinary skill in the art this claim.

Claim 54:

This application implements DirectX function in VSP hardware, VSPs 525 and 620 are external to the CPU 315, and DirectX has a DirectX Blend function. Column 34 line 61 to column 36 line 62 discusses implementing DirectX in hardware to relieve the CPU of graphics processing such as the DirectX Blend function.

Claim 22:

This claims a method claim version of system claim 41 and it is rejected for the reasons given for claim 1 above.

Claim 24:

Both figures 5 and 6 illustrate the north bridge of the single integrated circuit chip communicating between the CPU and the rest of the chip's internal components such as 525, 620.

Claim 26:

This claims a method claim version of system claim 5 and it is rejected for the reasons given for claim 5 above.

Claim 27:

This claims a method claim version of system claim 6 and it is rejected for the reasons given for claim 6 above.

Claim 30:

This claims a method claim version of system claim 9 and it is rejected for the reasons given for claim 9 above.

Claim 31:

This claims a method claim version of system claim 10 and it is rejected for the reasons given for claim 10 above.

Claim 32:

This claims a method claim version of system claim 11 and it is rejected for the reasons given for claim 11 above.

Claim 35:

This claims a method claim version of system claim 16 and it is rejected for the reasons given for claim 16 above.

Claim 36:

This claims a method claim version of system claim 17 and it is rejected for the reasons given for claim 17 above.

Claim 39:

This claims a method claim version of system claim 20 and it is rejected for the reasons given for claim 20 above.

Claim 51:

This claims a method claim version of system claim 50 and it is rejected for the reasons given for claim 50 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over So, U.S. Patent No. 5,909,559. Column 126 line 55 discusses MIPS processor but does not specifically mention SH3 processor and SH 4 processor. These two processors are SuperH RISC microprocessors from Hitachi. The MIPS microprocessor is another RISC microprocessor but from Silicon Graphics. It would have been obvious to one of

ordinary skill in the art to substitute one well known RISC microprocessor for another RISC microprocessor since they have similar capabilities, thus, the selection of which RISC microprocessor can be based upon economics at any one point in time.

7. Claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over So, U.S. Patent No. 5,909,559, in view of Yee et al., U.S. Patent No. 6,466,581.

These claims claim big endian and little endian. Before analyzing these claims it is important to define these terms which may be found in An Essay on Endian Order.

Copyright (C) Dr. William T. Verts, April 19, 1996.

Little endian definition:
"Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first.)
Intel processors (those used in PC's) use "Little Endian" byte order.
Big endian definition:
"Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address. (The big end comes first.)
Motorola processors (those used in Mac's) use "Big Endian" byte order.
The essay may be found at http://www.cs.umass.edu/~verts/cs32/endian.html

Another useful definition teaching a system that uses either type is from webopedia:

Many mainframe computers, particularly IBM mainframes, use a big-endian architecture. Most modern computers, including PCs, use the little-endian system. The PowerPC system is *bi-endian* because it can understand both systems
This definition may be found at http://www.webopedia.com/TERM/b/big_endian.html

Yee at column 4 lines 30-48 and column 7 lines 33-48, teach converting from little endian to big endian and from big endian to little endian at a PCI controller in order to allow a PowerPC to have access to peripheral devices such as a memory using different endian.

It would have been obvious to one of ordinary skill in the art at the time of applicants invention to incorporate little endian to big endian and from big endian to little endian conversion in the chip carrying the north gate function because this will allow the CPU to interface with diverse peripheral devices that do not use the same endian as the CPU.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jeddeloh, US Patent Nos. 6,157,398 and 6,947,050, teach a first main memory that is shared by CPU and graphics accelerator and a second main memory used by only CPU.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffery A Brier whose telephone number is (571) 272-7656. The examiner can normally be reached on M-F from 7:00 to 3:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi, can be reached at (571) 272-7664. The fax phone Number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffery A Brier
Primary Examiner
Art Unit 2672